Introduction

Micrel-Synergy's SY89429A frequency synthesizer is designed to be used in various clock subsystems. The Primary function of the product is to synthesize clock frequencies required for systems needing a high quality, low jitter clock source.

The cost of other clock sources, either crystal or SAW oscillators, increase dramatically as precision/frequency requirements of digital systems push into the 100+ MHz arena. Many low cost CMOS frequency synthesizers appeared in the market in the last few years. Unfortunately, these products have relatively high jitter and limited operating frequency range. Therefore, their applications are limited to lower precision/lower frequencies.

SY89429A, designed with Micrel-Synergy's high performance ASSET Bipolar technology and differential ECL circuit technology throughout, is a perfect low cost alternative to the expensive crystal or SAW oscillators. Unlike other frequency synthesizers, SY89429A has extremely low jitter and high supply noise rejection that ECL is famous for.

Because the device is programmable between 25MHz to 400MHz using a 16MHz crystal, different system frequency requirements can all use the same device. This may dramatically reduce inventory costs and management of additional products otherwise required to achieve these various frequencies. This programmability also makes board/system speed grading possible as part of the normal production flow without multiple oscillators. This provides higher overall yield and lower manufacturing cost.

In addition to cost savings, there are many other benefits to using SY89429A. Normal system production testing can incorporate frequency margining that is unavailable to fixed frequency designs as in crystal or SAW oscillators. This capability leads directly to higher product quality and reliability. Furthermore, SY89429A can be programmed in small steps (1MHz steps with a 16.000MHz crystal). Other precise frequencies can be programmed as well. See section titled "**Advance Frequency Control Applications**." This ability to provide any frequency eliminates the need for the high cost custom oscillator alternatives.

General Requirements

Operating the SY89429A is very simple. Very few low cost external components are required. These low cost external components provide the tuning capability needed to optimize and minimize jitter characteristics in each individual system application. To achieve the best possible performance in jitter and power supply noise rejection, basic high speed design guide lines should be followed.

Power Supply Requirements

SY89429A is designed to operate with a single +5V supply. The FOUT and /FOUT (the differential PECL outputs) will interface to PECL inputs of any +5 volt system. However, SY89429A can also be used in split supply (+5V and +3.3V) systems as well as true ECL systems. In a split supply application, the main V_{CC} lines, (V_{CC1}, V_{CC_QUIET}, and V_{CC_TTL}) are connected to +5V. The V_{CC_OUT} can be connected to either +3.3V or +5.0V. When applying +3.3V to V_{CC_OUT}, the differential PECL outputs will interface to PECL inputs of any +3.3V device. The GND and GND (TTL) pins are connected to the system ground in both cases. For split supply system, please refer to the section titled "**Split Supply Design**." For the ECL system, please refer to the section titled "**True ECL Design.**"

Power Supply Filtering Techniques

As in any high speed integrated circuits, power supply filtering is very important. A 0.1µF high frequency by-pass capacitor should be used between all separate power supply pins and ground. V_{CC1}, V_{CC_QUIET}, V_{CC_TTL} and V_{CC_OUT} should be individually connected to the power supply plane through vias, and a by-pass capacitor should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. In this case a ferrite bead along with a 1µF and a 0.01µF by-pass capacitor should be connected to each power supply pin. Figure 4 shows the connections of the power supply filtering using ferrite beads.

Termination For PECL Outputs

The differential PECL outputs, FOUT and /FOUT, are open emitter outputs. Therefore, terminating resistors or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize wave-form distortion. There are a few simple termination schemes. Figure 1 shows 3 simple termination circuits for a +5V system.

Interface For Inputs

The SY89429A is designed to interface with TTL compatible signals. All inputs except XTAL1 and XTAL2 are TTL compatible. These inputs have internal pull up resistors. Therefore, any inputs can be left open—open inputs are logical "1" state. Although inputs can be left open, it is recommended that open inputs be connected to a power supply line. These inputs can be connected to a power supply line (V_{CC} for a logical "1") or a ground line (V_{EE} for a logical "0") directly or through series resistors. Alternatively, these inputs can also be driven directly from any TTL compatible signals.

Input Reference Frequency And On-Chip Crystal Oscillator

The SY89429A is designed based on input reference frequency of 16MHz and phase detector frequency of 2MHz. A 16MHz differential PECL clock source can be used to drive the XTAL1 and XTAL2 pins directly. An alternative to a PECL clock source is to utilize the on-chip crystal oscillator. This oscillator requires only an off-chip 16MHz reference crystal connected between XTAL1 and XTAL2 pins. A 5.6kΩ resistor connected in parallel with the crystal is recommended. For using other input reference frequencies, refer to section titled "**Advance Frequency Control Applications**." Using 16MHz reference frequency, the output frequency can be programmed from 25MHz to 400MHz in 1MHz steps. Due to variability of the device, the crystal and the printed circuit board, connecting a fixed value capacitor in the 5-20pF range in series with the crystal should provide frequency control to 100ppm. Figure 3a shows the recommended crystal oscillator circuit. A variable capacitor can be used instead of the fixed capacitor to achieve frequency control better than 100ppm with manual adjustment. Varactors can also be included for using SY89429A as a voltage controlled oscillator. For more frequency control applications, please refer to the sections titled "**Advanced frequency control applications**" and "**Voltage controlled crystal oscillator applications**." For interfacing to TTL/CMOS clock sources, SY100ELT22 may be used to translate a TTL/CMOS signal to PECL signal.

Filter Design

The filter for any Phase Locked Loop (PPL) based device deserves special attention. SY89429A provides filter pins for an external filter. A simple three-components passive filter is recommended for achieving ultra low jitter. Figure 3b shows the recommended three-components passive filter. Due to the differential design, the filter is connected between LOOP_FILTER and LOOP_REF pins. With this configuration, extremely high supply noise rejection is achieved. It is important that the filter circuit and filter pins be isolated from any non-common mode coupling and placed in the V_{CC} plane.

Generating High Speed TTL Clock Signals

A high speed PECL-to-TTL translator such as SY10/100ELT23 or SY10/100ELT23L (for +3.3V) may be used to generate high speed TTL compatible signals. High speed PECL to TTL translating Clock Drivers such as SY10/100841/842 or SY10/100641/646 may be added if multiple copies of such clocks are desired. These translators are capable of driving 50pF loads up to 160MHz.

Split Supply Design

In systems where +5V are not available, a split supply design may be the solution. Split supply generally refers to using a positive supply and a negative supply to make up the total supply voltage. In the case of a +3.3V system, a –2V supply is needed to provide the required +5V across V_{CC} and V_{EE} terminals. Specifically, all V_{CC} pins including V_{CC_OUT} are connected to +3.3V supply. All ground pins are connected to –2V supply. This configuration eliminates the need for a +5V supply if there is a –2V supply already in the system. However, it also creates some interesting interface problems.

Since the most positive power supply is +3.3V, the XTAL1, XTAL2, FOUT and /FOUT interface to +3.3V PECL signal. If TTL interface is required, SY100ELT22L may be used at the XTAL1 and XTAL2 pins for translating the TTL signal to a +3.3V PECL signal. The SY100ELT23L can be used at FOUT and /FOUT pins for translating the +3.3V PECL signal to a TTL signal. Both SY100ELT22L and SY100ELT23L require only a single +3.3V power supply. Figure 5 shows a split supply design with TTL interface for XTAL1, XTAL2, FOUT and /FOUT.

Interfacing to all other inputs is trickier. As mentioned before, these inputs have internal pull up resistors. Therefore, any input can be left open and open inputs are logical "1" state. Although inputs are allowed to be open, it is recommended that open inputs be connected to a power supply line. These inputs can be connected to V_{CC} lines (+3.3V for a logical "1") or V_{EE} lines (–2V for a logical "0") directly or through series resistors. These inputs can also be driven by TTL or PECL signals with proper signal translators. Figure 6 shows the translation for a normal TTL signal. Figure 7 shows the translation for a +3.3V PECL signal.

True ECL Design

The SY89429A is designed for TTL/PECL systems. It can be designed into a pure ECL environment easily. Connect all V_{CC} pins to ground and all GND pins to –4.5V (or –5.2V) power supply line. With this operating condition, XTAL1, XTAL2, FOUT and /FOUT interfaces directly with normal 100K ECL signals. All other inputs have internal pull up resistors. Therefore, any input can be left open and open inputs are logical "1" state. Although inputs are allowed to be open, it is recommended that open inputs be connected to a power supply line. These inputs can be connected to ground lines (0 volt for a logical "1") or negative power supply lines (–4.5V or –5.2V for a logical "0") directly or through series resistors. These inputs can interface to normal ECL signals with SY100ELT23 for signal translation. Figure 8 shows the schematic with signal translations.

Advanced Frequency Control Applications

The primary function of this product is to synthesize clock frequencies from 25MHz to 400MHz in 1MHz steps with a 16.00MHz crystal. However, there are many other applications that are not so obvious. Even though SY89429A is said to be able to generate frequencies between 25MHz to 400MHz in 1MHz steps with a 16MHz crystal, output

frequency is programmed by properly configuring the internal dividers and can be represented by this formula (See Table 1 for an application example):

$$FOUT = \frac{FXTAL}{8} \times \frac{M}{N}$$

$$Step\ Size = \frac{FXTAL}{8} \times \frac{1}{N}$$

$$FVCO = \frac{FXTAL}{8} \times M$$

where

FXTAL is the crystal frequency or input reference frequency
M is the VCO frequency multiplier (from 2 to 511)
N is the post divider (2, 4, 8, or 16)
FVCO is the VCO frequency

Crystal oscillator frequency is designed to be less than 25MHz using a fundamental crystal. In many applications, wider range of input reference frequency can be used. Input frequencies at the low end is limited to above 6.26MHz due to minimum VCO frequency of 400MHz. Input frequency at the high end is limited by the speed of the phase detector and should not exceed 200MHz.

Frequency Multiplication Applications

As mentioned before, FOUT is a function of M and N. Therefore, output frequency may be set to any multiplication factor as long as the following is valid:

1) **M** is an integer between 2 to 511 inclusive
2) **N** is 2, 4, 8, or 16
3) Input reference frequency is more than 6.26MHz and less than 200MHz
4) **VCO** frequency is more than 400MHz and less than 800MHz

Using the FOUT equation, it is very easy to determine what M and N values must be for a certain multiplication factor.

One area of interest is communication. The frequencies often encountered are 155.52MHz for OC-3 or STS-3 and 51.84MHz for OC-1 or STS-1 standard SONET rates. The following table is a summary of how these frequencies may be generated:

Input Ref. Frequency	M	N	VCO	FOUT	Test (FOUT/4)
8.192MHz	405	8	414.72MHz	51.84MHz	12.96MHz
19.44MHz	256	4	622.08MHz	155.52MHz	38.88MHz
51.84MHz	96	4	622.08MHz	155.52MHz	38.88MHz
51.84MHz	96	8	622.08MHz	77.76MHz	19.44MHz

Table 1. M & N Combinations For Generating OC-3 and Related Frequencies

In addition to using a single SY89429A, multiple SY89429As in conjunction with dividers may be used to achieve multiple required frequencies. There are many companion divider products offered by Micrel-Synergy for these applications. SY100EL32 is a divider by 2 and SY100EL33 is a divider by 4. SY100S834 is a divider by 1, 2, 4 or 2, 4, 8 while SY100S838 is a divider by 1, 2/3 or 2, 4/6. Figure 9 and 10 show examples of using SY89429A in conjuction with dividers to generate all OC-3 and related frequencies using 19.44MHz and 16.384MHz clock, respectively. The MR (Master Reset) pins are used to synchronize all frequency outputs.

Voltage Controlled Crystal Oscillator Applications

SY89429A is a PLL (Phase Locked Loop) based frequency synthesizer with on chip crystal oscillator. With a 16MHz crystal connected in series with varactors as shown in Figure 11, the oscillator frequency can easily be pulled by ±1000ppm. Since the output frequency is directly proportional to the cyrstal oscillator frequency, the output frequency is pulled by the same amount (in ppm) as the crystal oscillator.

Pulse Shaping Application

For applications where 50% duty cycle clock is important, SY89429A may be the perfect solution. Many clock Oscillators or signals from the back plane do not provide the required 50% duty cycle. The problem may be corrected by simply using the SY89429A as a 1X frequency multiplier. The FOUT output will always maintain 50% duty cycle. However, phase relationship between the input and output may not be maintained. For frequencies between 25MHz and 200MHz, use the SY89429A as a 1X multiplier. For frequencies between 200MHz and 400MHz, use a divide by 2 stage as a prescaler and the SY89429A as a 2X frequency multiplier as shown in Figure 12.

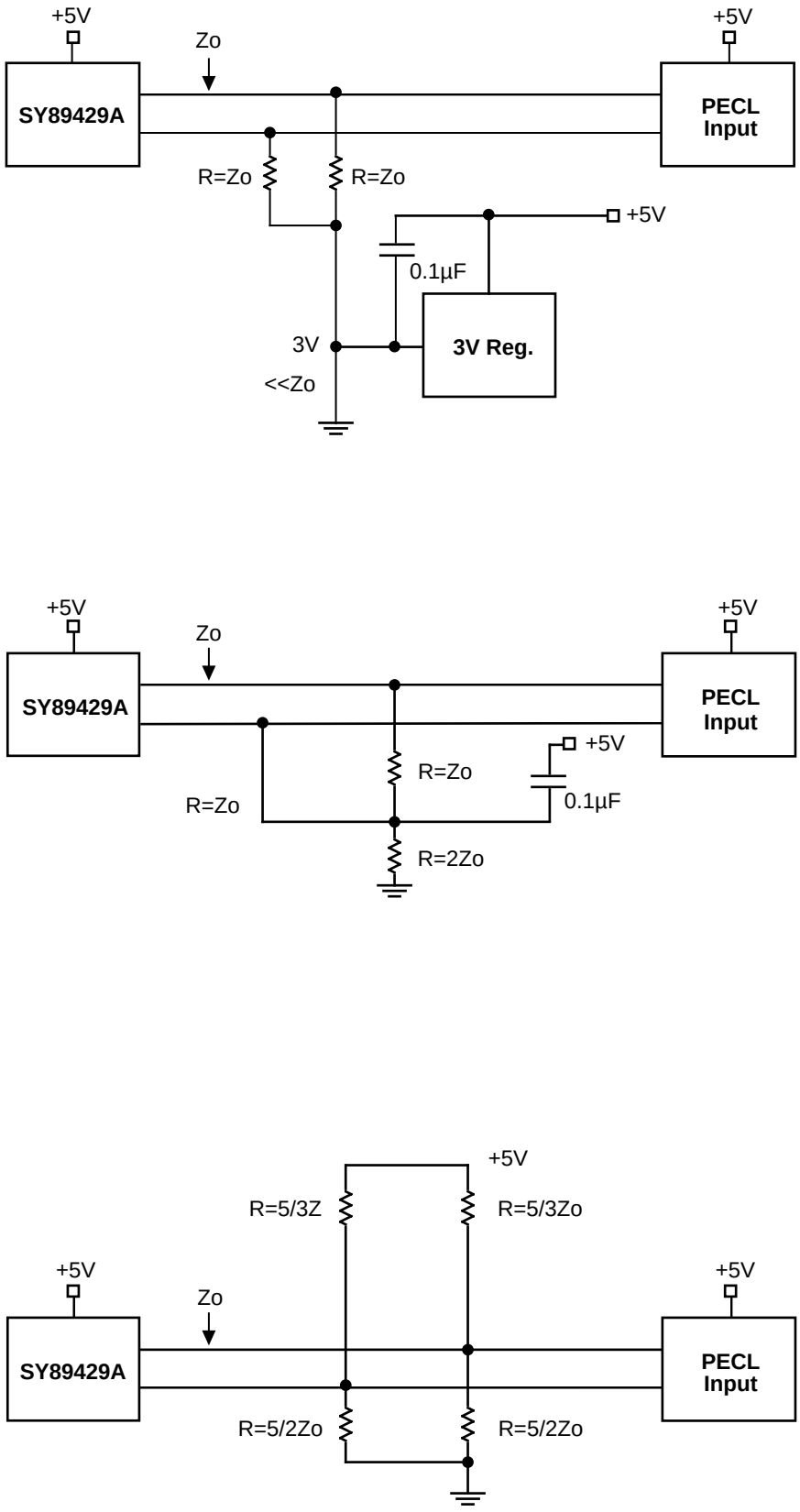


Figure 1. Matched Impedance Termination Schemes for 5V Systems

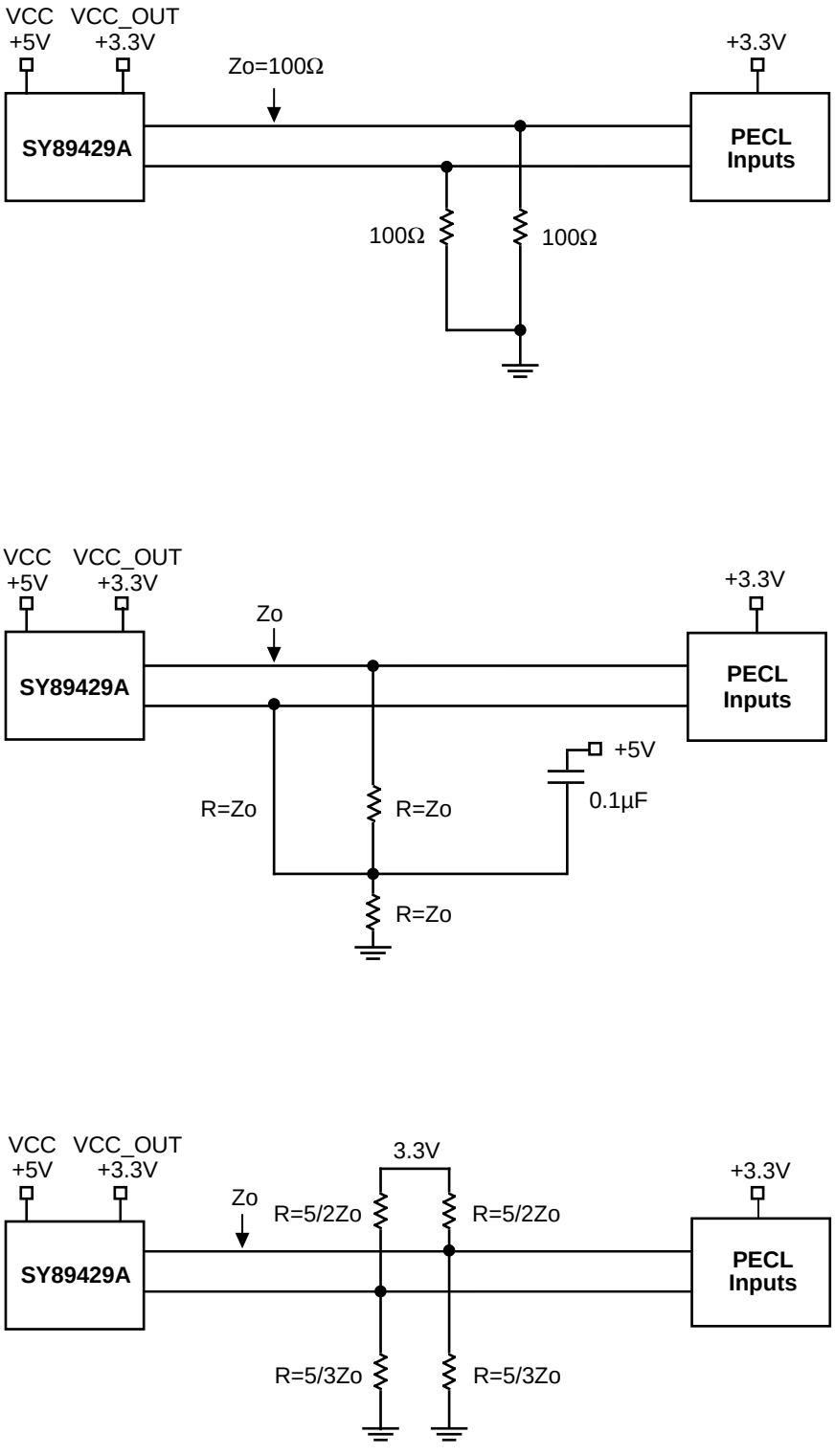


Figure 2. Matched Impedance Termination Schemes for Split 5V and 3.3V Systems

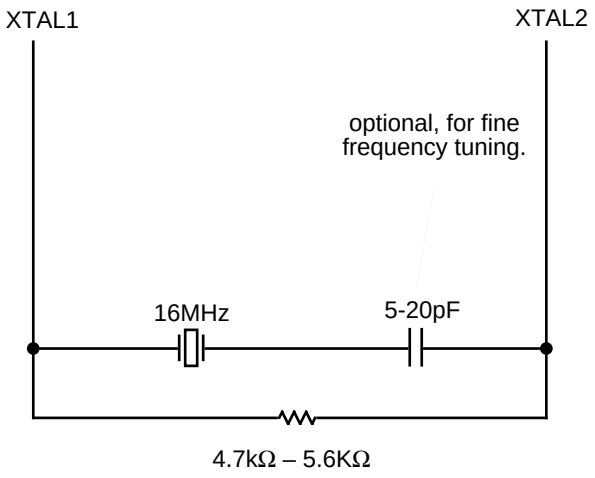


Figure 3a. Recommended External Components for Crystal Oscillator

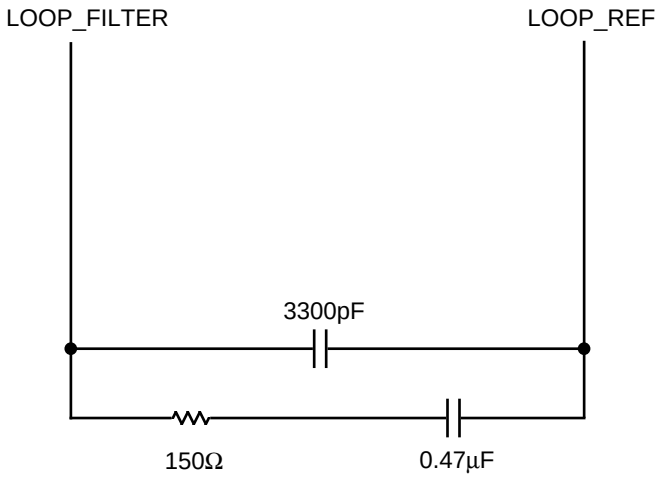


Figure 3b. Recommended Passive Filter Circuit

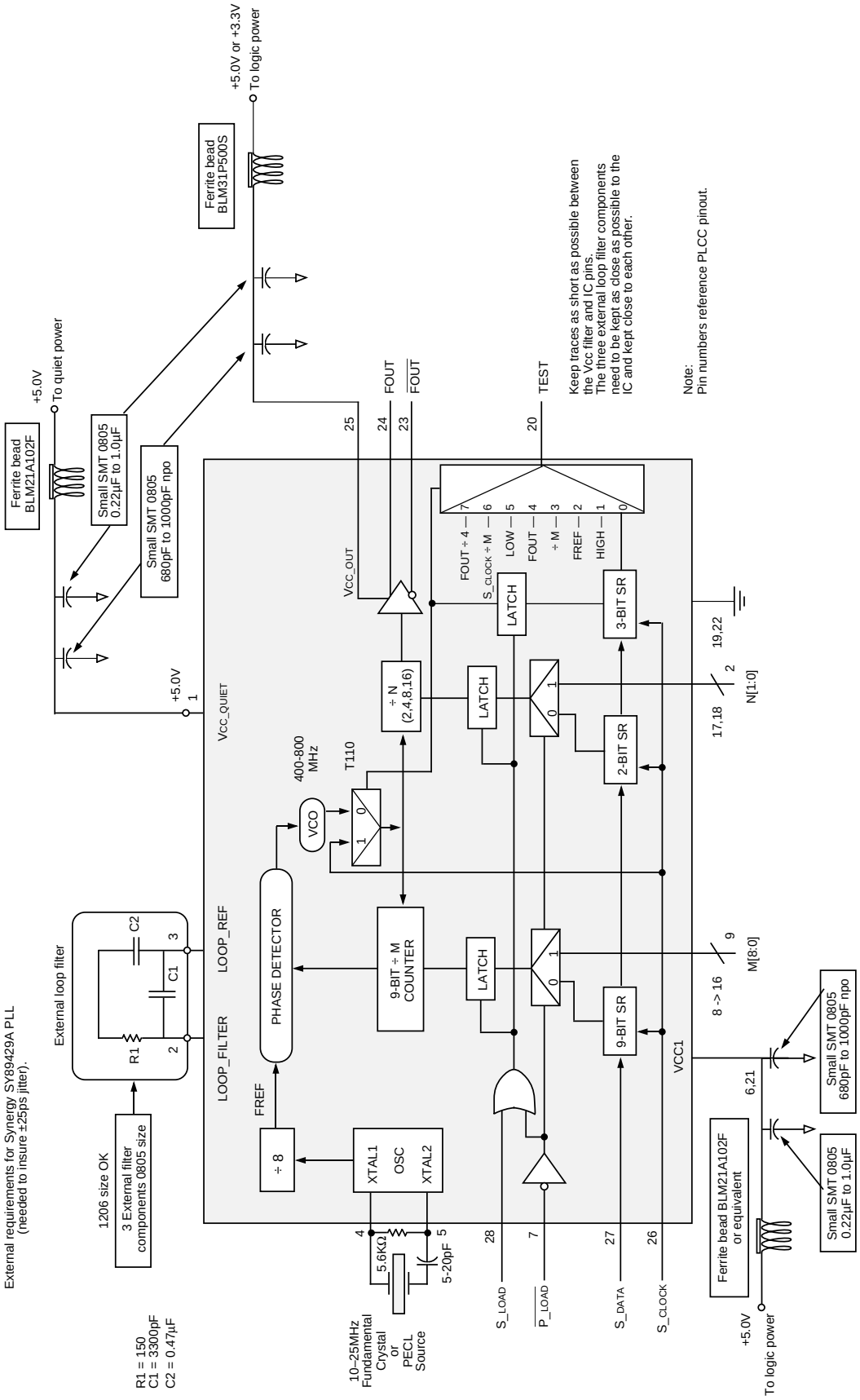


Figure 4. Power Supply Filtering

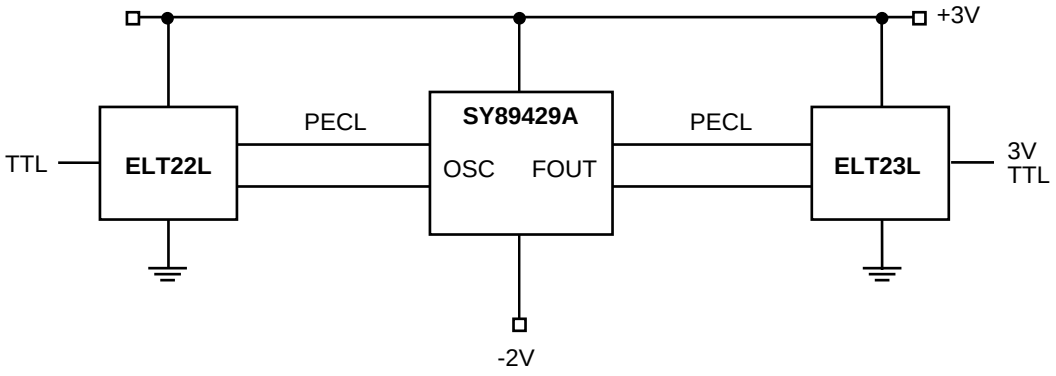


Figure 5. Split Supply Designs

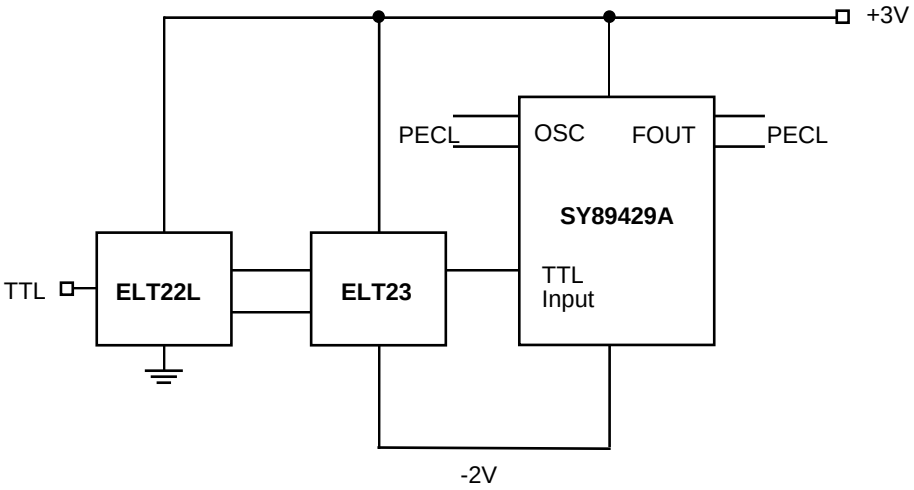


Figure 6. Interfacing to SY89429A TTL Inputs with 3V TTL Signals for Split Supply Designs

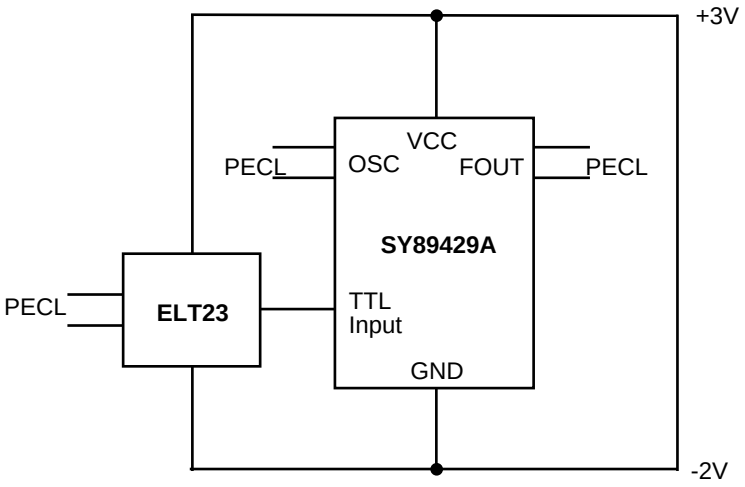


Figure 7. Interfacing to SY89429A TTL Inputs with 3V PECL Signals for Split Supply Designs

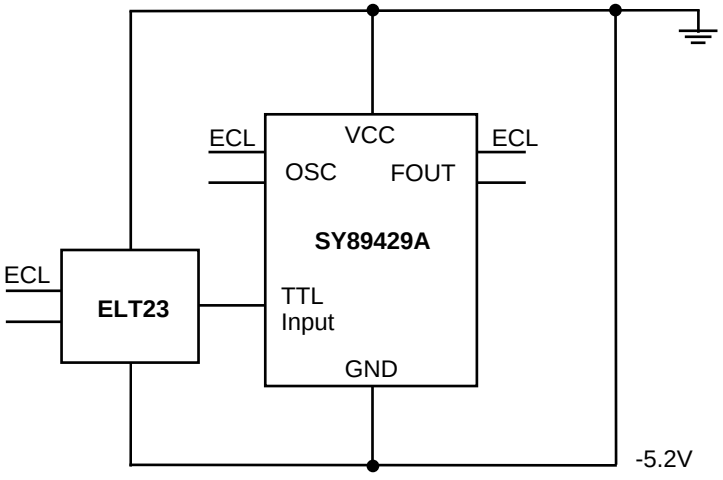


Figure 8. Interfacing to SY89429A TTL Inputs with ECL Signals for True ECL Designs

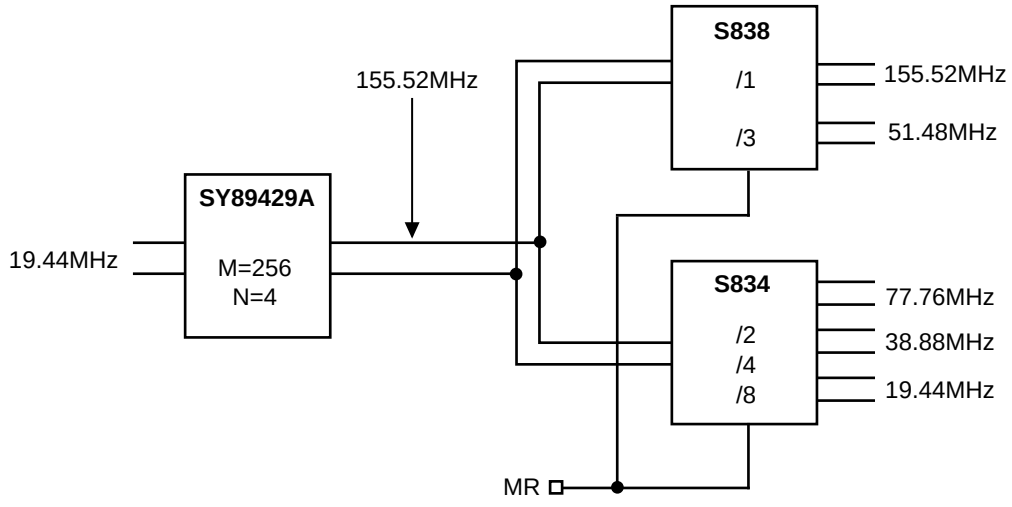


Figure 9. Generating OC-3 and Related Frequencies using 19.44MHz Reference

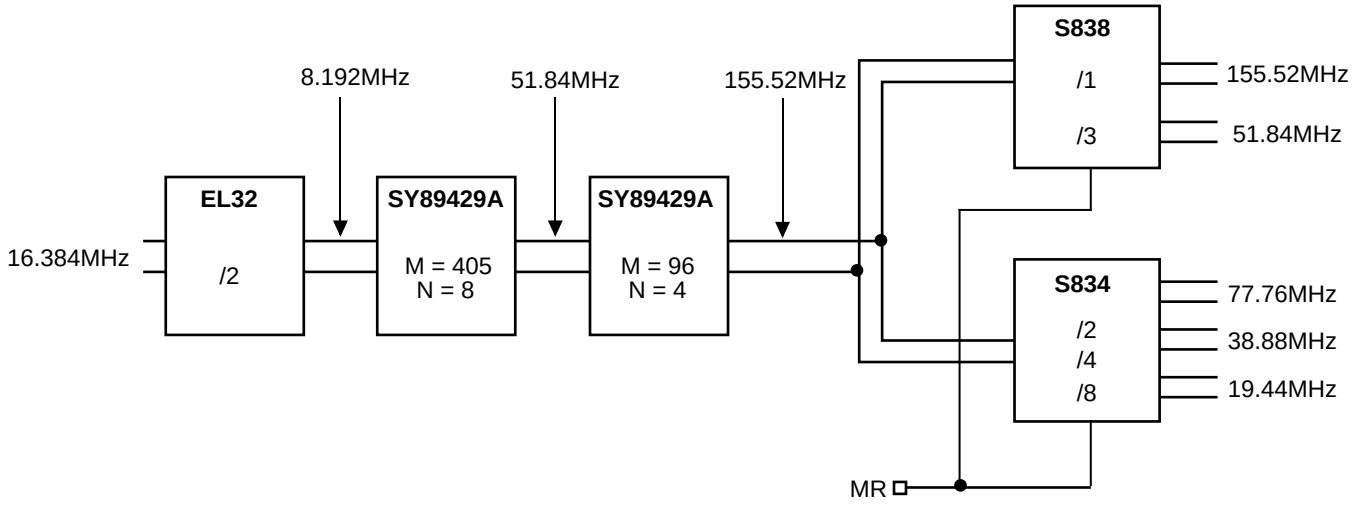


Figure 10. Generating OC-3 and Related Frequencies using 16.384MHz Reference

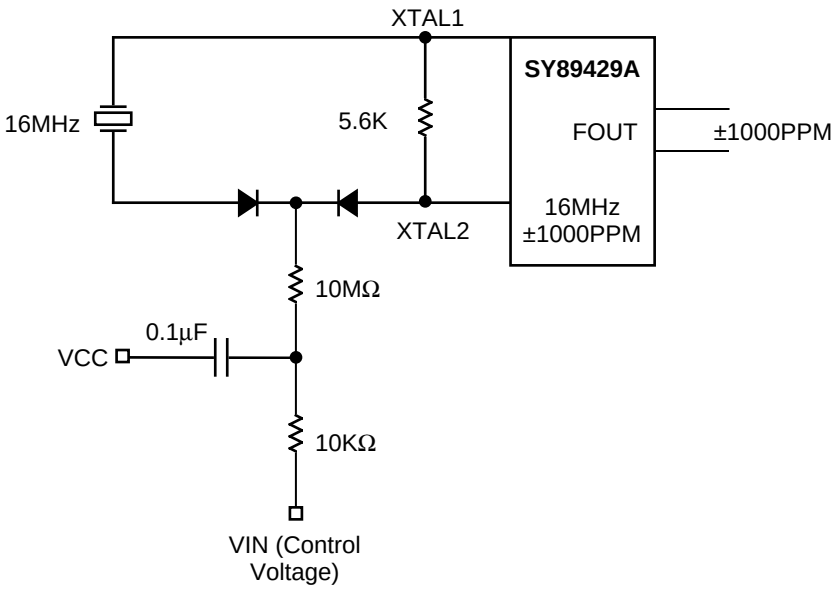
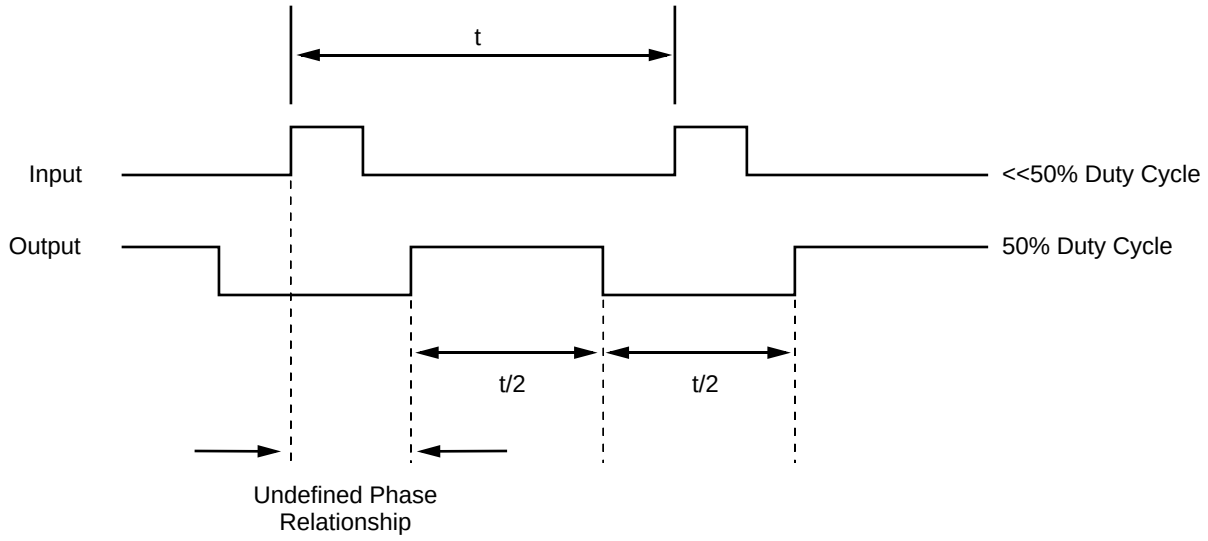
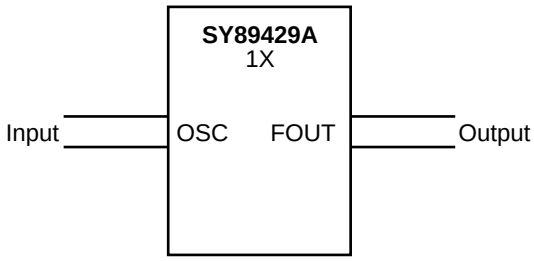
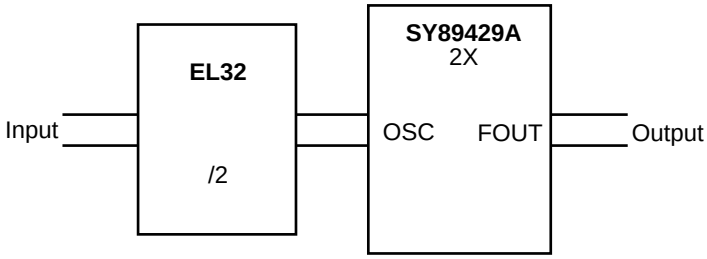


Figure 11. Voltage Controlled Crystal Oscillator Cicuit (VCXO)





For Frequencies Between 25MHz and 200MHz



For Frequencies Between 25MHz and 200MHz

Figure 12. 50% Duty Cycle Pulse Shaping Circuits